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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/663,967	09/16/2003	Hyun-Chul Kim	5649-1161	2684

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MYERS BIGEL SIBLEY & SAJOVEC
PO BOX 37428
RALEIGH, NC 27627

EXAMINER	
GUERRERO, MARIA F	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 06/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/663,967	KIM, HYUN-CHUL
	Examiner	Art Unit
	Maria Guerrero	2822

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *9-25* is/are pending in the application.

4a) Of the above claim(s) *17-25* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *9-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is in response to the Election and the amendment filed April 14, 2005.

Status of Claims

2. Claims 1-8 are canceled. Claims 9-25 are pending.

Election/Restrictions

3. Applicant's election of Species I (claims 9-16) in the reply filed on filed April 14, 2005 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Claims 17-25 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on filed April 14, 2005.

Information Disclosure Statement

4. The information disclosure statements filed September 16, 2004 and October 14, 2003 have been considered.

Priority

5. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Specification

6. The disclosure is objected to because of the following informalities: in page 6, lines 5 and 14, the specification recites "as illustrates in Figure 1A, a substrate **100**".

Appropriate correction is required.

The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 9-16 are rejected under 35 U.S.C. 102(b) as being anticipated by Shih et al. (US 6,100,118).

8. Shih et al. shows forming an integrated circuit device (col. 6, lines 35-45). Shih et al. teaches forming a window layer on an integrated circuit substrate that defines a fuse region (Figs. 1-4, col. 6, lines 35-67). Shih et al. describes the window layer being formed at an upper portion of the integrated circuit device and recessed beneath a surface of the integrated circuit device (Figs. 1-4, col. 7, lines 54-60). Shih et al.

discloses forming a buffer pattern between the integrated circuit substrate and the window layer (Figs. 1-4, col. 4, lines 20-60). Shih et al. shows forming a fuse pattern comprising a first conductive material between the buffer pattern and the window layer (Figs. 1-4, col.4).

9. In addition, Shih et al. teaches forming a metal wiring on the integrated circuit substrate being more remote from the integrated circuit substrate than the window layer (Figs. 1-4, col. 6, lines 15-45). Shih et al. shows forming the buffer pattern by forming a first buffer pattern, a second buffer pattern, a first insulation layer between the first buffer pattern comprising a second conductive material and the fuse pattern, and a second insulation layer between the second buffer pattern comprising a third conductive material and the first buffer pattern (Figs. 1-4, col. 4, col. 7, lines 1-60). Shih et al. describes the window layer being formed by forming a third insulation layer on the first insulation layer, forming a passivation layer on the third insulation layer, and etching the passivation layer and the third insulation layer in the fuse region (Figs. 1-4, col. 4, lines 15-65, col. 7, lines 52—60, col. 8, lines 44-67, col. 9, lines 1-5).

10. Shih et al. also teaches the second and the third conductive materials are different from the first conductive material (col. 3, lines 40-65, col. 7, lines 10-14, 45-48). Shih et al. shows the first and second buffer pattern being planar (Figs. 1-4). Shih et al. describes forming a line pattern between the integrated circuit substrate and the second insulation layer adjacent the second buffer pattern (Figs. 1-4, col. 4). Shih et al. teaches forming a contact hole in the first and second insulation layers that exposes a portion of

the line pattern and forming a contact plug in a contact hole that electrically couples the fuse pattern to the line pattern (Fig. 1-4, col. 4, lines 15-60).

11. Furthermore, Shih et al. discloses forming a conductive layer pattern between the second insulation layer and the first insulation layer adjacent to the first buffer pattern (Figs. 1-4, col. 4, lines 15-55). Shih et al. teaches forming a metal wiring on the third insulation layer above the conductive layer pattern and forming a via hole in the first and third insulation layers that exposes at a portion of the conductive layer pattern and forming a conductive plug in the via hole that electrically couples the conductive patter and the metal wiring (Figs. 1-4, col. 4, lines 5-65, col. 11, lines 17-28). Shih et al. shows the integrated circuit device comprises an integrated circuit memory device (col. 1, lines 12-15, col. 6, lines 43-45).

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Billig et al. (US 5,025,300), Lee et al. (US 6,448,113), Huang et al. (US 6,121,073), Tsai (US 6,295,721), Mori et al. (US 6,713,837), Bae (US 6,716,679), Bae (US 6,573,125), Kim et al. (US 6,642,135) describe several embodiments related to applicant's disclosure.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Maria Guerrero whose telephone number is 571-272-1837.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

June 15, 2005

MARIA F. GUERRERO
PRIMARY EXAMINER